REMARKS

Claims 1, 2, 5, and 7-10 have been amended. No new matter has been added. Claims 1-10 remain in the application. Reconsideration and reexamination is respectfully requested.

There are two common usages for the word "stale" in relation to data in a cache memory. In a first usage, the word means that the data has not been used recently. See, for example, U.S. Patent Number 6,134,634 cited in the present application. In a second usage, the word means that the data is obsolete (that is, there is a newer value available for the data). In the present application, the word "stale" is used for data that has not been used recently. Applicant submits that amendments to the claims are not necessary in light of the prior art. However, for purposes of clarity, claims 1, 2, 5, and 7-10 have been amended to clarify that the word "stale" refers to data that has not been recently accessed. No new matter has been added. Support for the amendments may be found, for example, in the abstract (last sentence) and in the summary (page 4, lines 4-7).

In paper 3, claims 1-10 were rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent Number 5,655,103 (Cheng *et al.*). Applicant respectfully traverses.

Claim 1 specifies a cache memory. The cited stale bits in Cheng *et al.* are in a memory controller, not a cache (see, for example, column 5, lines 10-11 and lines 27-28.

Claim 1 specifies that each age bit is in the same structure as the corresponding data (both are in a cache memory). In Cheng *et al*, the stale bits are in the memory controller, and the corresponding data values are in a cache.

Claim 1, as amended, specifies that the age bits indicate whether corresponding data has been recently accessed. In Cheng *et al*, the stale bits are not used to indicate whether corresponding data has been recently accessed.

Claim 7 specifies setting a bit to a first logical state when the entry is accessed. Access can occur without a miss. That is, when the data is in the cache, reads and writes do not result in a miss. In Cheng *et al.*, the stale bit is set to the first logical state when an entry in the dependency table is created, and entries in the dependency table are created

PAGE 9/10 * RCVD AT 6/10/2004 10:42:21 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:970 898 7247 * DURATION (mm-ss):02-38

only when a Load Miss occurs (see, for example, abstract; figure 2; column 2, lines 22-33; column 5, lines 10-13; column 5, lines 39-40).

Claim 7, as amended, specifies determining that an entry has not been recently accessed when the bit is at the second logical state for at least a predetermined time. In Cheng *et al*, the stale bits are not used to indicate whether corresponding data has been recently accessed.

The above remarks in conjunction with claim 7 apply equally to claims 8 and 9. Claim 8 specifies setting a bit to a first logical state when the entry is written. Writing can occur without a miss. Claim 9 further specifies that the bit corresponds to an index. In Cheng *et al*, there is no correspondence between stale bits and indexes.

Claim 10 specifies that the age bit is used to determine that is an entry is dirty and has not been recently accessed. In Cheng *et al*, the stale bits are not used to indicate whether corresponding data has been recently accessed.

The following comments are in regard to other art made of record by the examiner.

U.S. Patent Numbers 5,671,391, 6,026,475, 6,425,057, 6,490,671, 6,493,801, 6,542,861, 6,678,794, and U.S. Patent Publication Number US 2002/0078303 do not teach or suggest a cache memory including age bits indicating whether entries have been recently accessed, as specified in claim 1, or determining that an entry has not been recently accessed when a bit is at the second logical state after at least a predetermined time after being set to the second logical state, as specified in claims 7-10. .

Entry of this amendment is respectfully requested. This application is considered to be in condition for allowance and such action is earnestly solicited.

Respectfully submitted,

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